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Comparative THD Analysis of Multilevel Inverter using level shift PWM schemes

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Abstract:

In medium power and high voltage application Multilevel Inverter are used. Because of its simple design and ease of implementation, the level shift PWM scheme is primarily used for pulse generation. For pulse generation, IPD, POD, and APOD MCPWM techniques are discussed. This paper uses MATLAB simulation to discuss the comparative analysis of harmonics. The MLI CHBMLI topology is used for discussion.The CHBMLI topology of MLI is preferred over other topologies due to its lower power semiconductor components, cost, and size. THD percentage is discussed and compared for various levels of output voltage waveform. When compared with other schemes for the identical level of output voltage, the IPD scheme has the lowest THD. The output waveform becomes smoother and more sinusoidal as THD decreases.

Keywords: *Multilevel Inverter, Level Shift PWM scheme, IPD, POD, APOD Modulation Scheme*

1 Introduction

In new cascaded switch-ladder MLI topologies, decreases switch count and gives more no of output voltage level and voltage rating of components is discussed in [1]. Different MLI topologies and its application is discussed in [2]. Three-phase CHBMLI topology with abate power electronic components and hybrid control technique to produce gate pulses for switches are discussed in [3]. Cascaded H-bridge MLI topology with different control techniques for output voltage level generates less THD is discussed in [4]. A self-balanced step-up MLI topology to reduce total standing voltage and PIVfor switches are discussed in [5]. Different reduced switch MLI topologies gives higher voltage levels to improve power quality and reduces filter requirements are discussed in [6]. A new three-phase modular multi-level inverter (MMLI) topology using both SPWM and staircase modulationstechniques generate output voltage levels with lessen switch count, voltage stress and harmonic distortion than other MLI topologies are discussed in [7]. New cascade MLI topology generating both even and odd voltage levels at output with lessen power electronic components and cost by using extended sub multilevel units which connected in series are discussed [8]. A novel MLI topology using sinusoidal pulse width modulation techniques to generate gate pulses and filters to reduce THD are discussed in [9]. The advantages of multilevel inverter and various compromises for reducing power semiconductor components are discussed in [10]. The novel unified power flow controller (UPFC) with cascaded H-bridge MLI offers many advantages and applications than conventional configuration is discussed in [11]. To obtain high power and medium voltage application modified three-phase multilevel inverter configuration using PWM technique is discussed in [12]. Cascaded MLI giving positive and negative voltage level at output by using different algorithm is discussed in [13]. Symmetric MLI with reduced switch count, cost and loss compared to cascaded H-bridge MLI generates higher levels of output voltage are discussed in [14]. In MLI SHEPWM techniques diminishes more THD value related to ordinary PWM techniques are discussed in [15]. A new MLI topology using in-phase disposition (IPD) SPWM techniques for high voltage and high-power application is discussed in [16-17]. Modern advancement in MLI topologies, modulation and control techniques are discussed in [18]. Symmetric and asymmetric topologies of MLI producing all levels of output voltage with reduction in switches, cost and size are discussed in [19]. A current control algorithm with discrete time model for CHBMLI generating all levels of output voltage are discussed in [20]. Particle swarm optimization (PSO) method to solve harmonic elimination problems with unequal dc sources in cascaded H-bridge MLI are discussed in [21]. Series connection of CHB cells with photovoltaic (PV) module for MPPT is discussed in [22]. The three-phase configuration of CHBMLI circuits and various forms of multi carrier sinusoidal

PWM (MCSPWM) are discussed in [23]. Emerging topologies, the most important methods of control and modulation, and recent MLI applications are discussed in [24].

2. CHBMLI

Full form of CHBMLI is Cascade H-bridge Multi level inverter.7-level CHBMLI is depicted in below figure contains four switches in each H-bridge cell. When 'K' H-bridges are linked in series, a maximum KE output voltage of 2K+1 separate output voltage level is obtained, where E is input voltage of single H-bridge. When K=3, the output vol. has 7-levels 3E, -3E,2E, -2E, E, -E and 0 respectively. Switching table for 7-level output waveform is given in Table1. For E=50v, output voltage waveform for 7-level CHBMLI using IPD, POD & APOD scheme is in Fig-2, Fig-3& Fig-4 respectively.

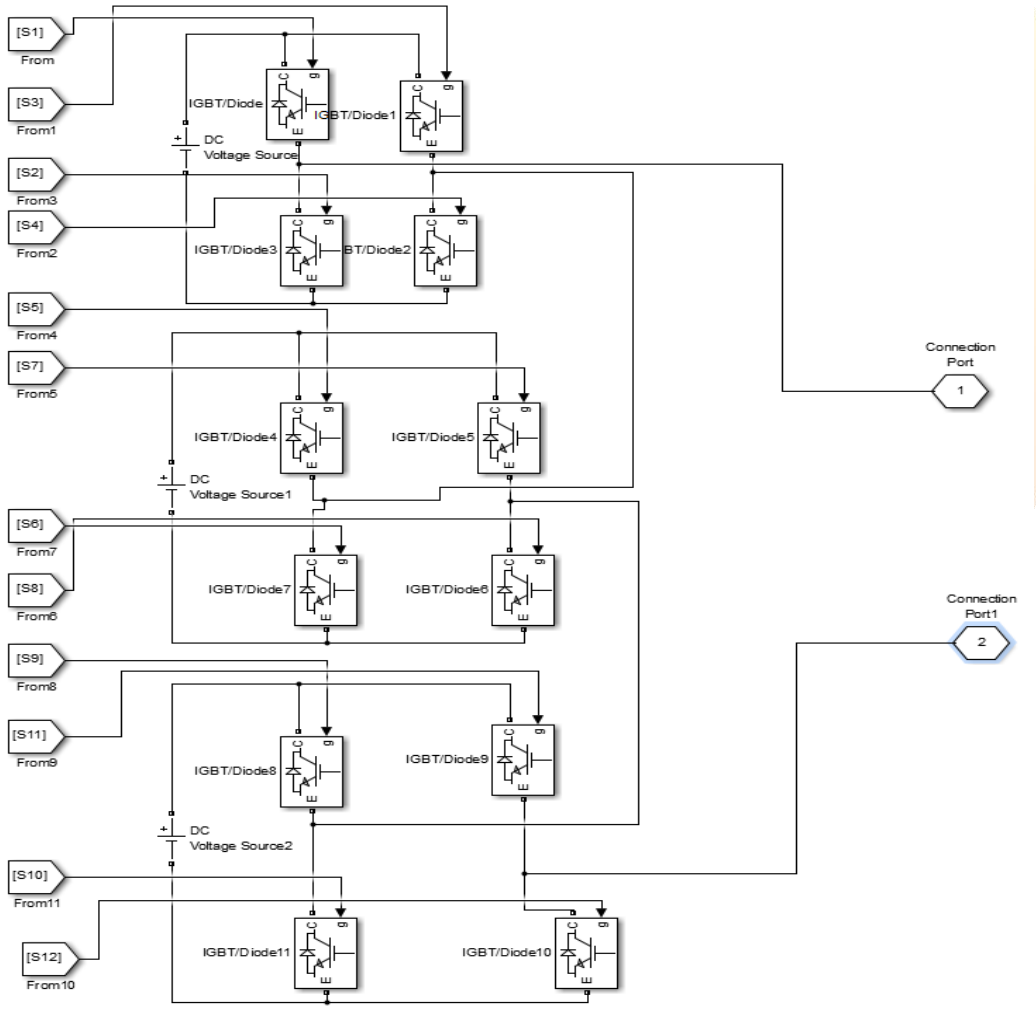


Fig-1.Circuit for 7-level CHBMLI

Table 1 Switching table for7-level CHBMLI

Voltage levels	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12
3.0E	1	0	0	1	1	0	0	1	1	0	0	1
2.0E	1	0	0	1	1	0	0	1	1	0	1	0
E	1	0	0	1	1	0	1	0	1	0	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0
-E	0	1	1	0	1	0	1	0	1	0	1	0
-2.0E	0	1	1	0	0	1	1	0	1	0	1	0
-3.0E	0	1	1	0	0	1	1	0	0	1	1	0

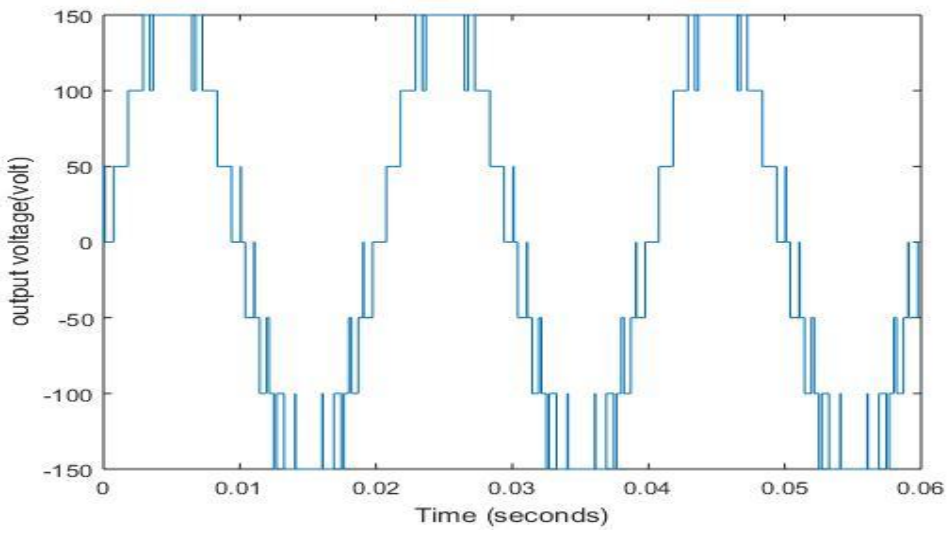


Fig-2.7 level output voltage using IPD scheme

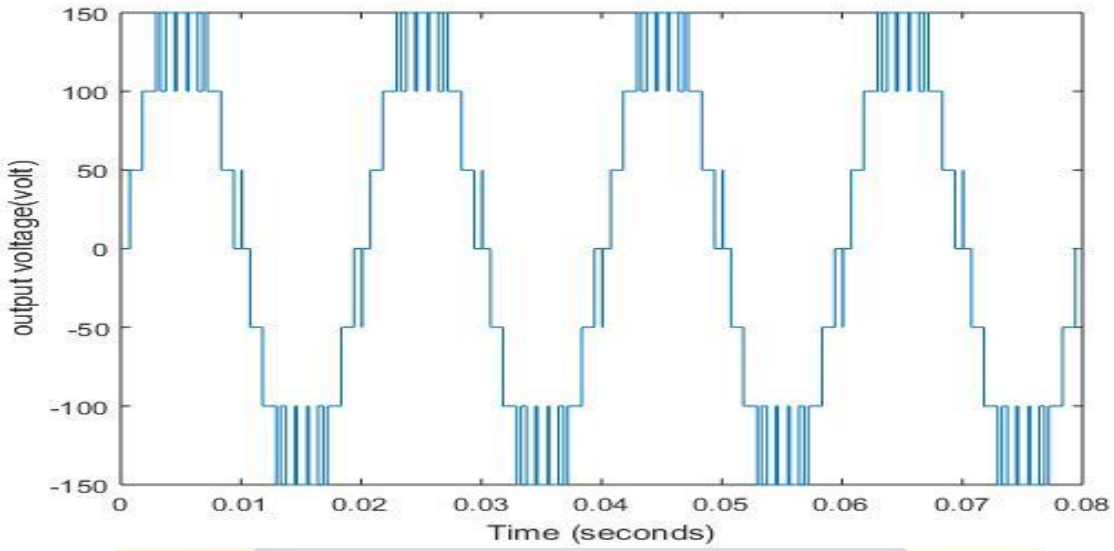


Fig-3.7 level output voltageusing POD scheme

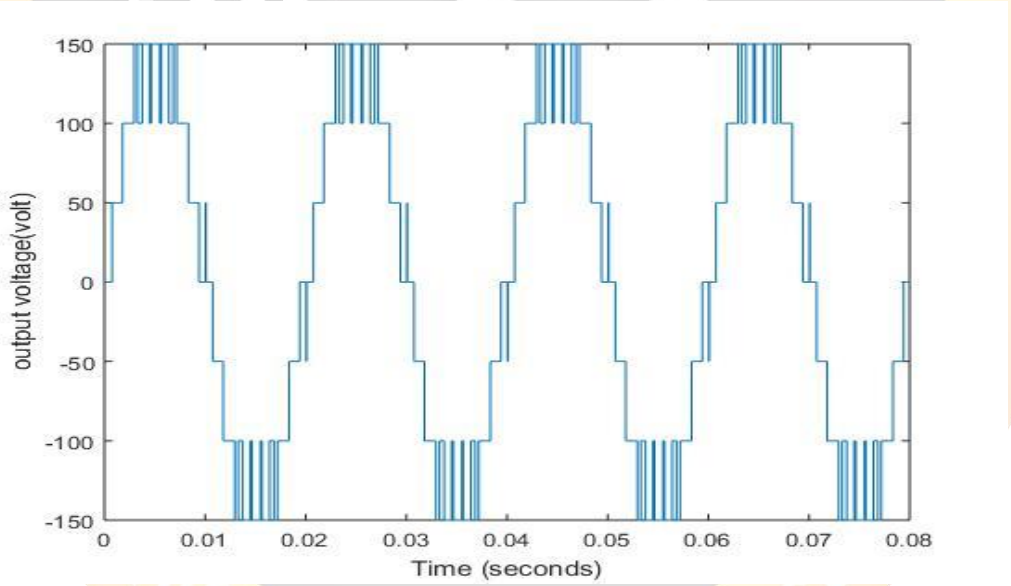


Fig-4.7 **Level Output Voltage Using APOD Scheme**

3. Sinusoidal PWM scheme for Inverter

PWM (Pulse width modulation) is the inverter's internal control tool. A low frequency sinusoidal reference wave is proportional to the high frequency triangular (Δ) carrier wave, to produce gate pulses for switches.

Output pulses are not identical i.e., they are having the variable width of pulses. The width of pulse varies in accordance with the magnitude of sinusoidal waveform. Pulses are generated using SPWM scheme and provided to switches for unalike output voltage levels. THD percentage for distinct output voltage levels are discussed and compared in table below.

Table 2 THD percentage for different levels of output voltage

No. of Levels	THD Percentage (%)
3	55.88
5	26.89
7	16.45
9	16.79
11	14.04
13	8.58

4. Level Shift PWM scheme for inverter

To get output waveform with reduced harmonic contents of MLI, it is necessary to implement a proper modulation technique. MCPWM scheme is one of the best methods of pulse generation for switches due to simple architecture and simpler implementation. In MCPWM scheme, the reference wave is a sinusoidal signal and the carrier wave is a triangular signal. A multi-level inverter with'm' voltage levels includes '(m-1)' triangular (Δ) carriers. The identical frequency and peak-to-peak amplitude are used for all triangular (Δ) carriers. The Gate signals are generated when reference signal is collate with the carrier signal.

MCPWM Schemes are categorized as level shifted, phase shifted and hybrid PWM. Level shifted PWM is of three types which is In-phase disposition (IPD), Phase opposite disposition (POD) and Alternative phase opposite disposition (APOD). In IPD, signal is in phase for all carriers. In POD,

all carriers below the zero reference are opposite in phase and all carriers above zero reference are in phase. Every carriers shows opposite disposition alternatively in APOD.

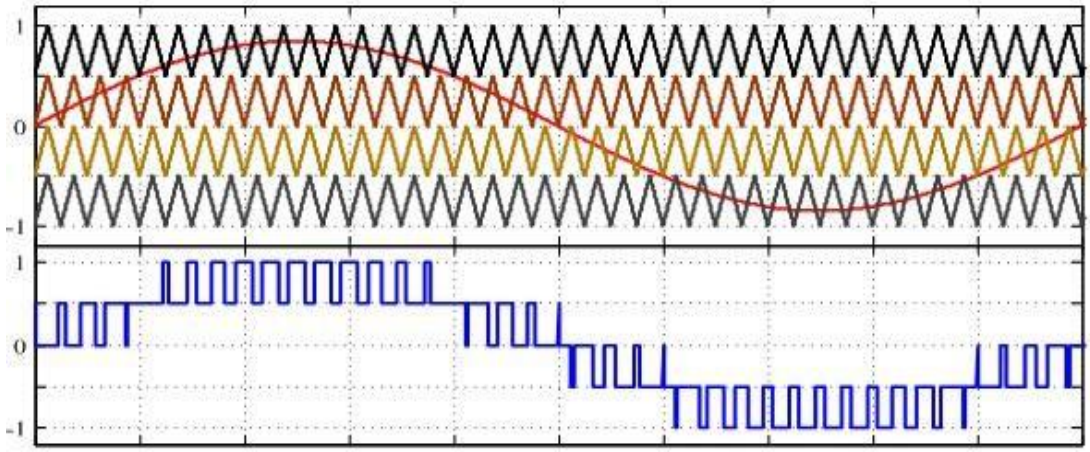


Fig-5.IPD Modulation Scheme

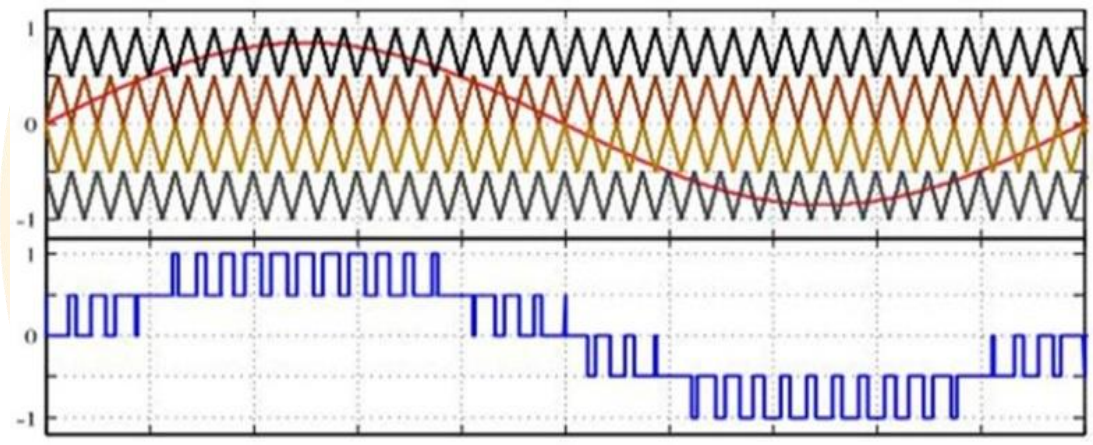


Fig-6. POD Modulation Scheme

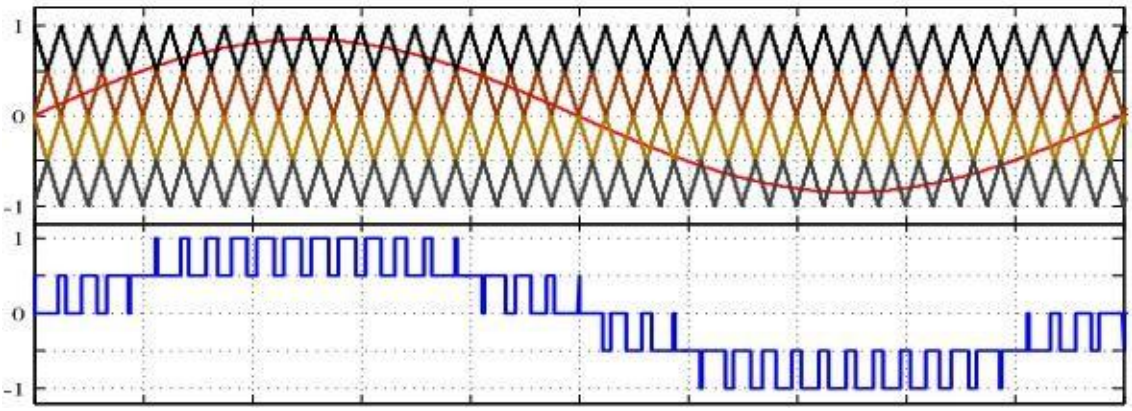


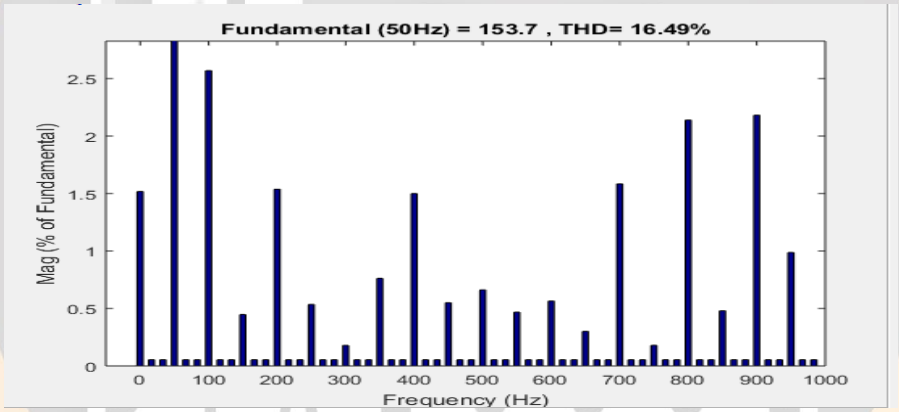
Fig-7. APOD Modulation Scheme

5.Benefits of IPD Modulation Technique

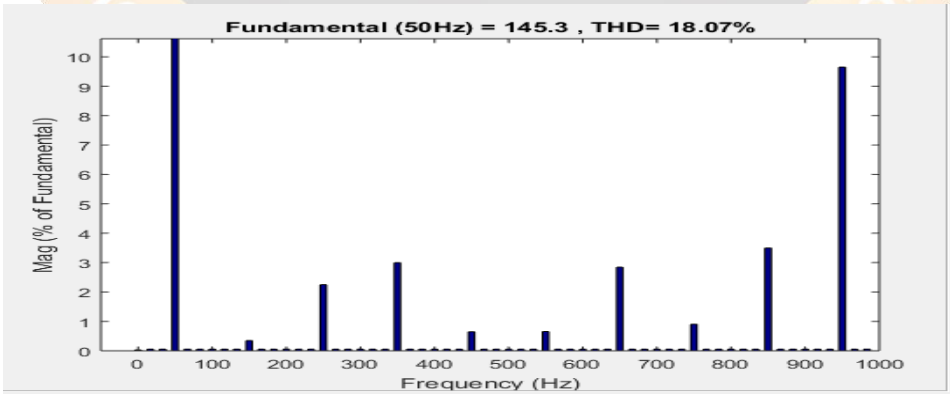
In this scheme, the line voltage is reduced because thecarrier frequency harmonics are made as carrier frequency common mode voltage and thus gets cancelled out in line voltage. It is advantage over POD and APOD techniques. This approach is valid for all types of multi-level inverter.

6. Simulation result

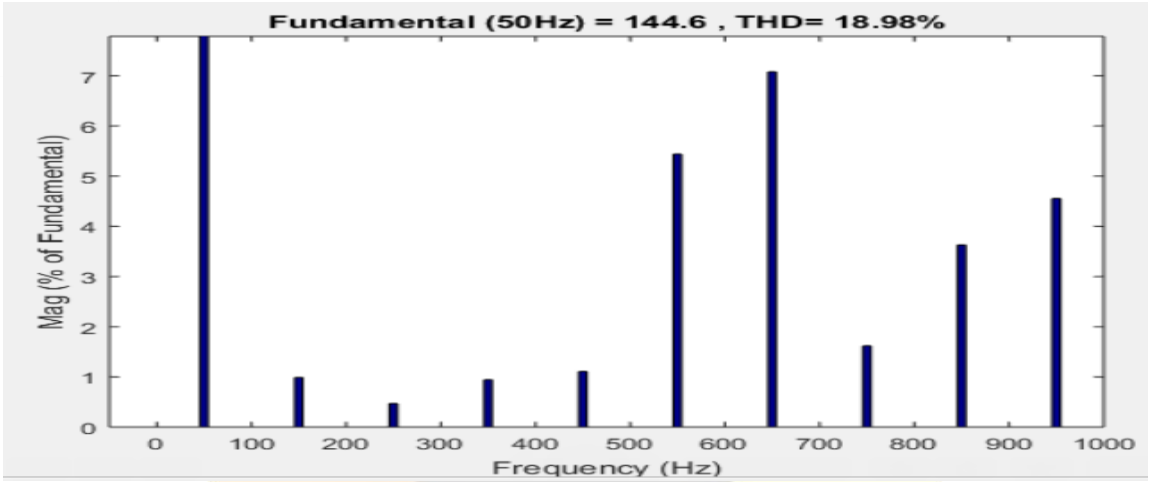
The simulation result using MATLAB technique is discussed in the present paper. Thecarriersignal frequency is 1KHz and reference signalfrequency is 50Hz. Thegate pulses for the switches of CHBMLI are generated by comparingsinusoidal reference signal and triangular (Δ) carrier signal. The THD% of 7 levels CHBMLI using IPD, POD and APOD PWM schemes is shown in graph below. In IPD scheme THD is 16.49%. In POD scheme THD is 18.07%. In APOD scheme THD is 18.98%.



Graph-1. THD of 7-level CHBMLI using IPD scheme



Graph-2. THD of 7-level CHBMLI using POD scheme



Graph-3. THD of 7-level CHBMLI using APOD scheme

Table 3 THD percentage of different level output vol.

No. of Levels	THD%		
	IPD	POD	APOD
3	53.21	55.87	54.03
5	24.98	26.89	28.16
7	16.49	18.07	18.98
9	12.94	17.59	15.37
11	10.31	10.55	12.16
13	8.92	9.37	9.67

7. Conclusion

IPD, POD and APOD schemes which is based on level shift PWM has been effectivelyapplied for different levels of output voltage in CHBMLI. THD percentages for these different levels are depicted in Table 3. THD percentage for different levels of output vol. using SPWM schemes are depicted in Table 2. From the abovetable-2and table-3, we observe that with rise of number of levels, reduce the percentage of THD(THD%). Among all level shift PWM schemes, IPD has the lowest THD% for same level output voltage.

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